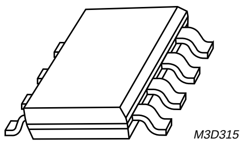


PHK12NQ03LT

TrenchMOS™ logic level FET

Rev. 01 — 22 March 2002 **Product data**

1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™[1]technology.

Product availability:

PHK12NQ03LT in SOT96-1 (SO8).

1.2 Features

- Low on-state resistance
- Fast switching

1.3 Applications

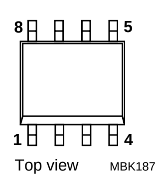
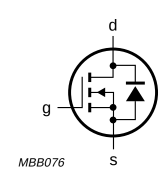
- DC to DC converters
- Portable equipment applications

1.4 Quick reference data

- V_{DS} = 30 V
- I_D = 12 A
- P_{tot} = 2.5 W
- R_{DSon} = 14 mΩ

2. Pinning information

Table 1: Pinning - SOT96-1, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	 SOT96-1 (SO8)	
4	gate (g)		
5,6,7,8	drain (d)		

1. TrenchMOS is a trademark of Koninklijke Philips Electronics N.V.

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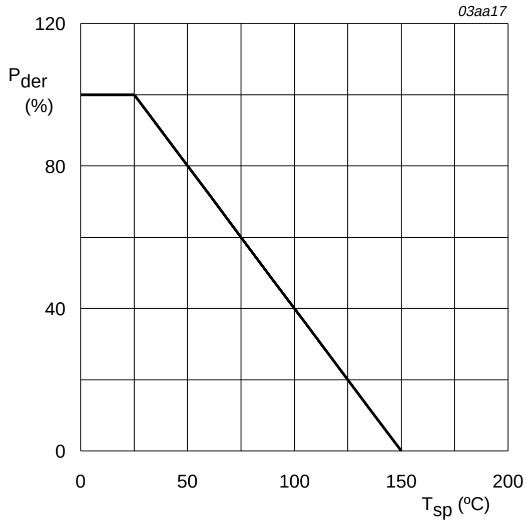
3. Limiting values

Table 2: Limiting values

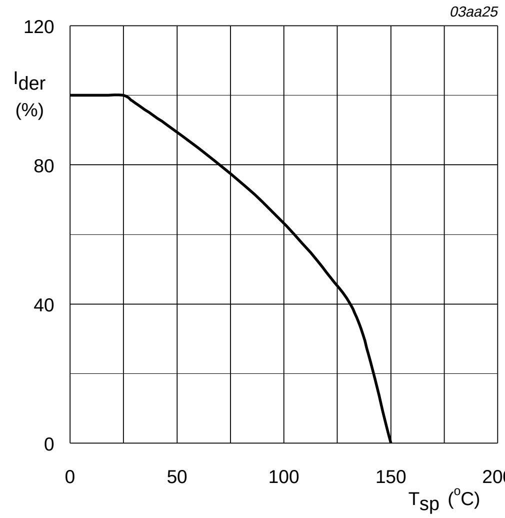
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	T_j = 25 to 150 °C	-	30	V
V_{GS}	gate-source voltage		-	±20	V
I_D	drain current	T_{sp} = 25 °C; Figure 2 and 3	-	12	A
I_{DM}	peak drain current	T_{sp} = 25 °C; pulsed; Figure 3	-	45	A
P_{tot}	total power dissipation	T_{sp} = 25 °C; Figure 1	-	2.5	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source (diode forward) current	T_{sp} = 25 °C	-	12	A



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

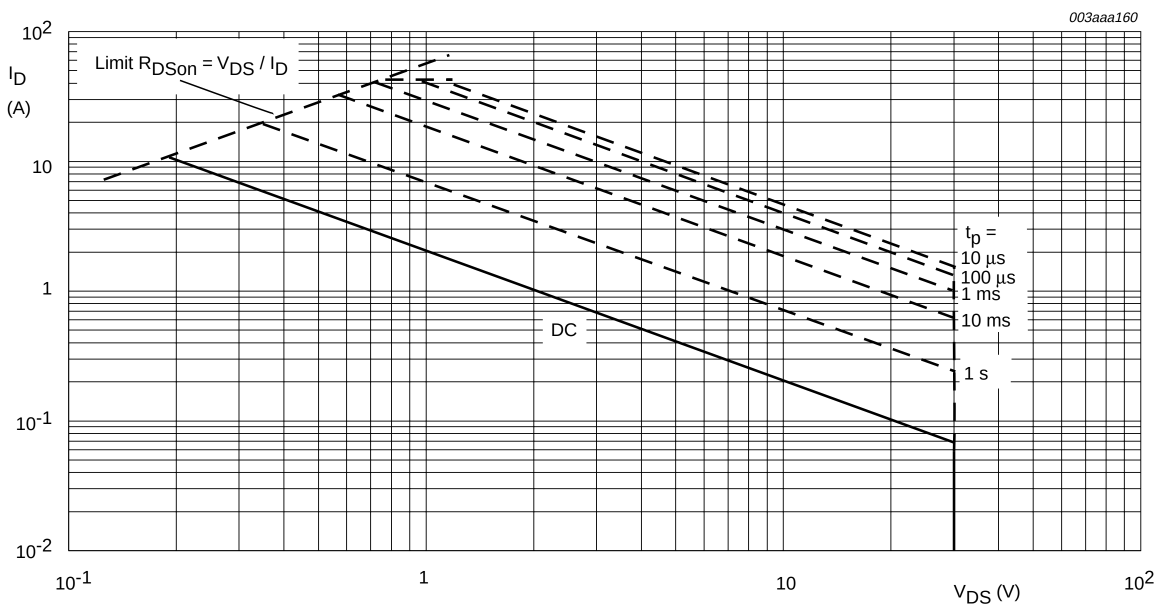
Fig 1. Normalized total power dissipation as a function of solder point temperature.



$V_{GS} \geq 5$ V

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



$T_{sp} = 25$ °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

4. Thermal characteristics

Table 3: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed circuit board; $t_p \leq 10$ s; minimum footprint; Figure 4	-	60	-	K/W

4.1 Transient thermal impedance

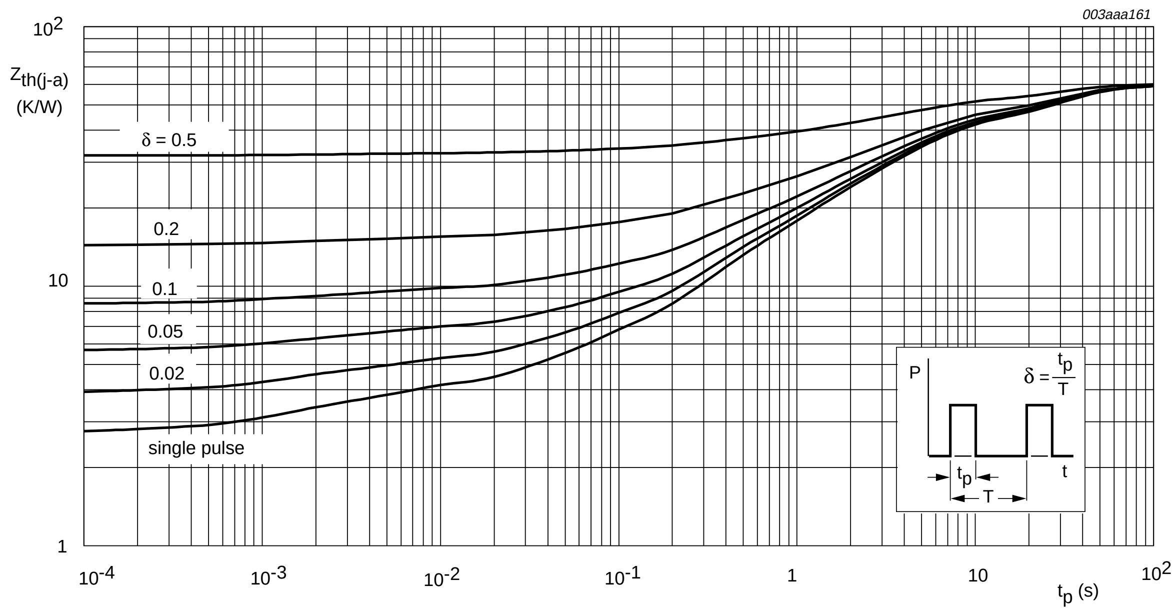


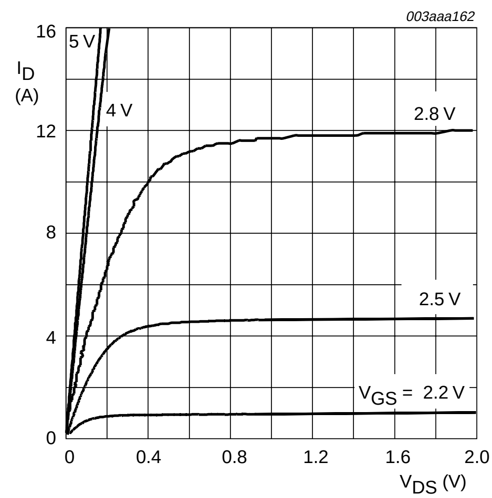
Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration.

5. Characteristics

Table 4: Characteristics

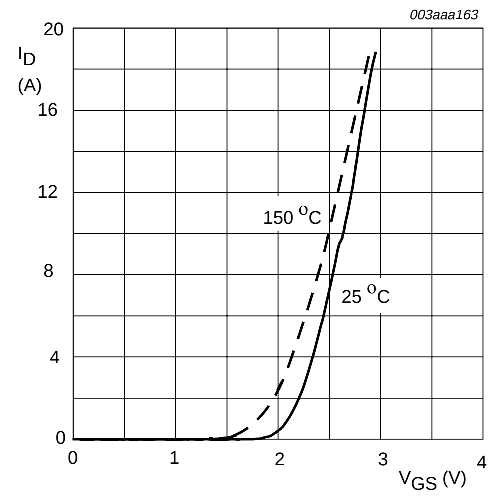
T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V	30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 250 µA; V_{DS} = V_{GS}; T_j = 25 °C; Figure 9	1	-	2	V
I_{DSS}	drain-source leakage current	V_{DS} = 24 V; V_{GS} = 0 V				
		T_j = 25 °C	-	-	1	µA
		T_j = 100 °C	-	-	5	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	-		100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 10 A; Figure 7 and 8	-	11	14	mΩ
		V_{GS} = 10 V; I_D = 12 A; Figure 7 and 8	-	8.9	10.5	mΩ
Dynamic characteristics						
g_{fs}	forward transconductance	V_{DS} = 15 V; I_D = 10 A;	-	34	-	S
$Q_{g(tot)}$	total gate charge	I_D = 15 A; V_{DD} = 16 V; V_{GS} = 5 V; Figure 13	-	17.6	-	nC
Q_{gs}	gate-source charge		-	4	-	nC
Q_{gd}	gate-drain (Miller) charge		-	4.4	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 16 V; f = 1 MHz; Figure 11	-	1335	-	pF
C_{oss}	output capacitance		-	391	-	pF
C_{rss}	reverse transfer capacitance		-	190	-	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 16 V; R_D = 10 Ω; V_{GS} = 10 V	-	10.6	-	ns
t_r	rise time		-	11.7	-	ns
$t_{d(off)}$	turn-off delay time		-	37	-	ns
t_f	fall time		-	19	-	ns
Source-drain (reverse) diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 1 A; V_{GS} = 0 V; Figure 12	-	0.7	1.0	V
t_{rr}	reverse recovery time	I_S = 2.3 A; dI_S/dt = –100 A/µs; V_{GS} = 0 V	-	70	-	ns



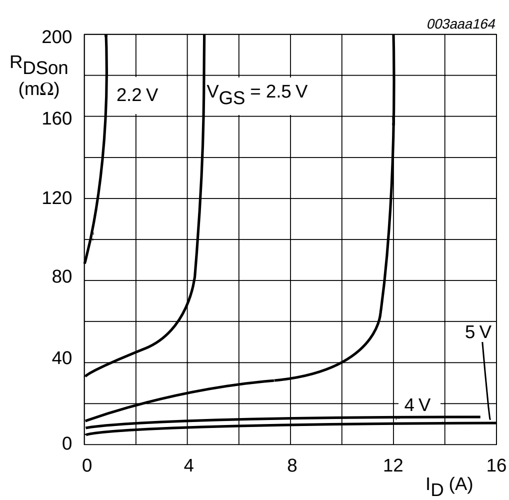
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



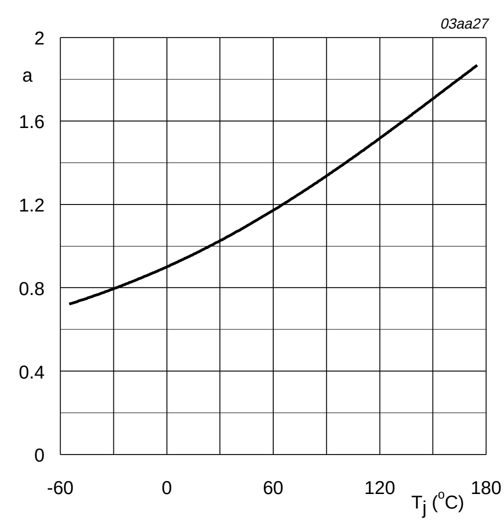
T_j = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



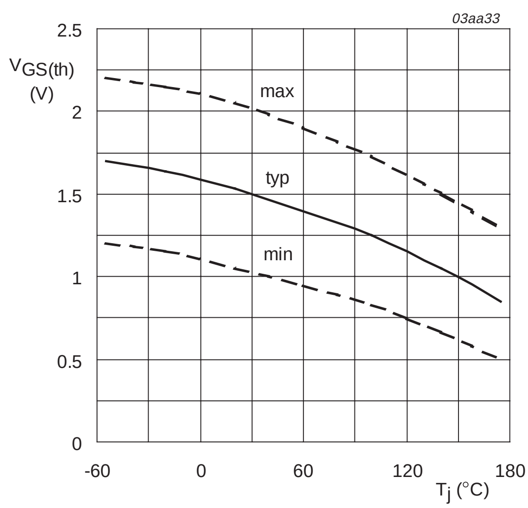
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



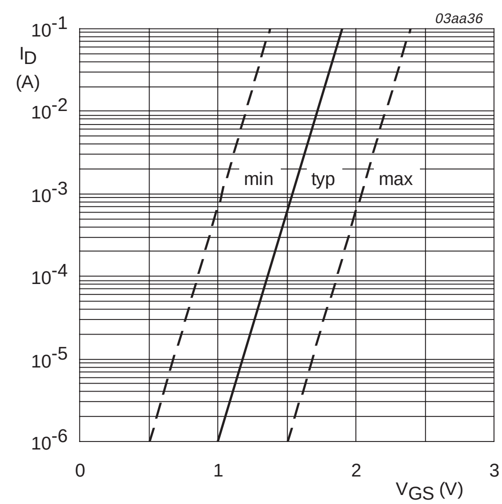
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 8. Normalized drain source on-state resistance factor as a function of junction temperature.



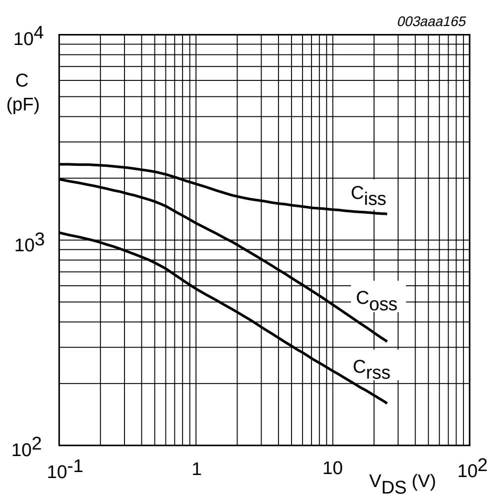
I_D = 1 mA; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



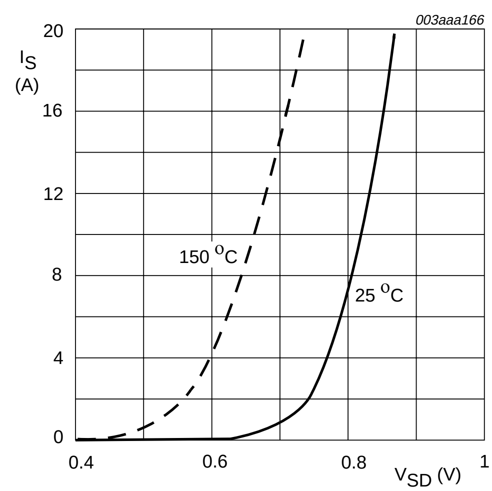
T_j = 25 °C; V_{DS} = 5 V

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



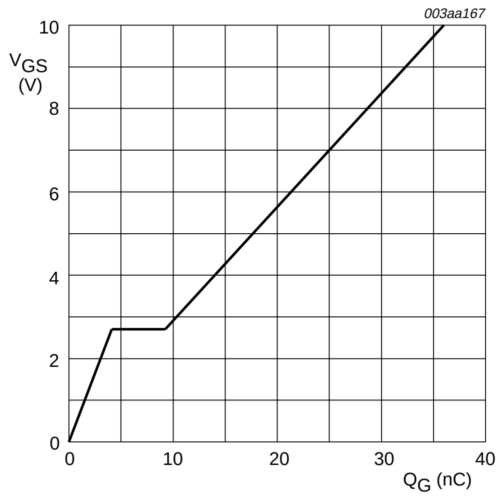
V_{GS} = 0 V; f = 1 MHz

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



T_j = 25 °C and 150 °C; V_{GS} = 0 V

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

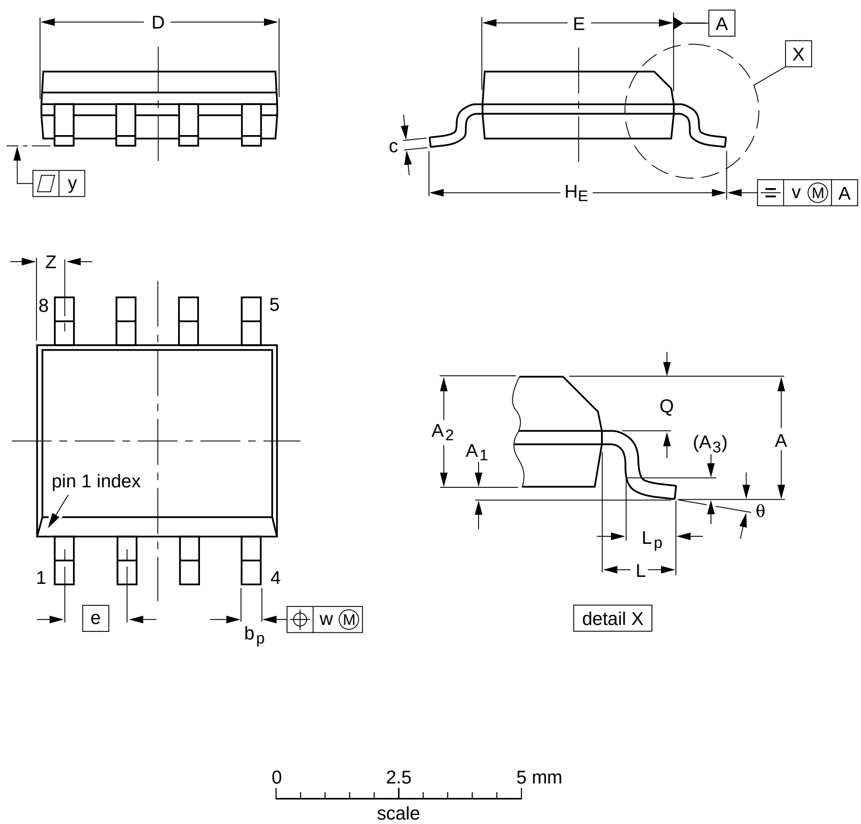


I_D = 15 A; V_{DD} = 16 V

Fig 13. Gate-source voltage as a function of gate charge; typical values.

6. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~95-02-04~~ 97-05-22

Fig 14. SOT96-1 (SO8).

7. Revision history

Table 5: Revision history

Rev	Date	CPCN	Description
01	20020322	-	Product data; initial version

8. Data sheet status

Data sheet status[1]	Product status[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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Contents

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